CS4461

Multi-Bit A/D for Class-D Real-Time PSR Feedback

Features

- Advanced Multi-bit Delta-Sigma Architecture
- Real-time Feedback of Power Supply Conditions (AC and DC)
- Filterless Digital Output Resulting in Very Low Signal Delay
- 135 mW Power Consumption
- Supports Logic Levels Between 3.3 V and 5.0 V
- Differential Analog Architecture
- Modulator Overflow Detection
- Interfaces Directly to the CS44800/CS44600 Class-D PWM Modulator
- Multi-bit Conversion at up to 7.5 MHz
- Delivers Modulated Data Over 2-Wire Interface

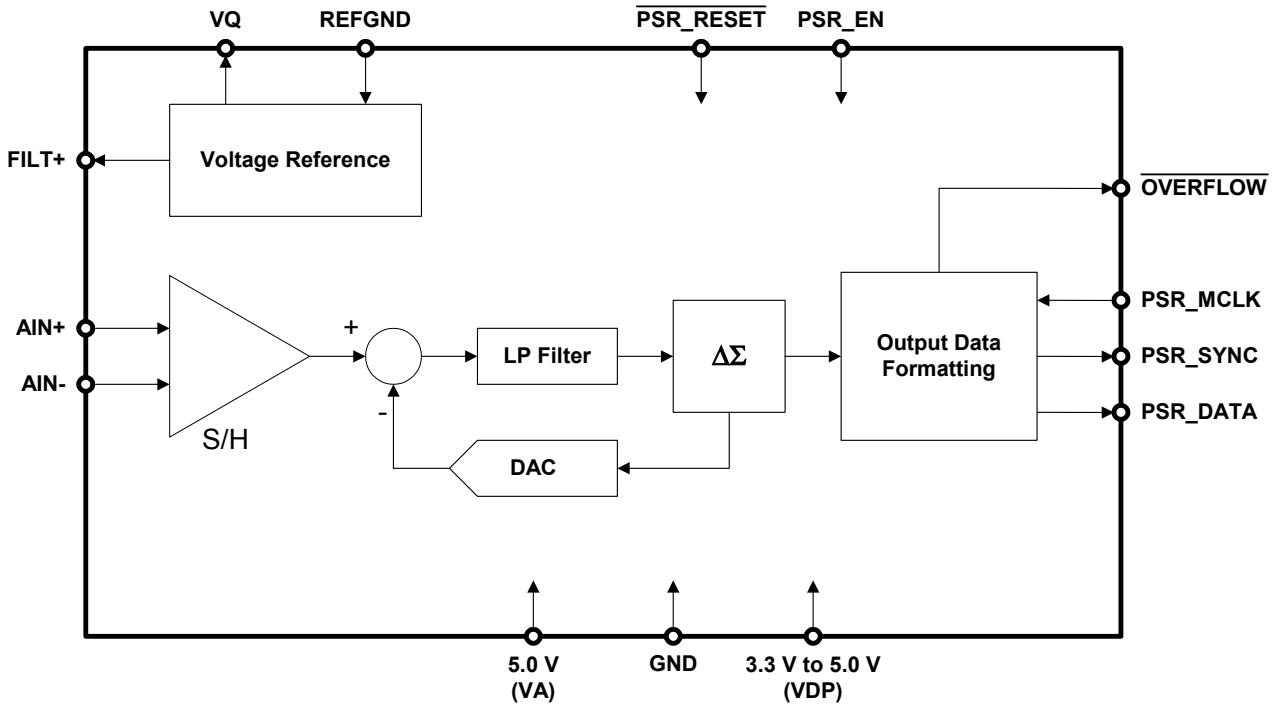
General Description

The CS4461 is a complete analog-to-digital converter for class-D real-time power supply rejection (PSR) feedback. It performs sampling and analog-to-digital conversion, generating digital data for input to a class-D modulator with real-time PSR feedback capabilities.

The CS4461 uses a 5th-order, multi-bit delta-sigma modulator followed by output data formatting. The ADC uses a differential architecture which provides excellent noise rejection.

The CS4461 feeds back the AC and DC voltage components and is ideal for class-D audio systems requiring high power supply rejection.

The CS4461 is available in a 24-pin TSSOP package in both Commercial (-10° to +70° C) and Automotive grade (-40° to +85° C). The CDB44800 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 11 for complete details.



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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:	Positive Analog	VA	4.75	5.0	5.25	V
	Positive Digital	VDP	3.1	3.3	5.25	V
Ambient Operating Temperature	Commercial (-CZZ)	T_{AC}	-10	-	+70	°C
	Automotive (-DZZ)	T_{AA}	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V, All voltages with respect to ground.) (Note 1)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Digital	VDP	-0.3	+6.0	V
Input Current	(Note 2)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 3)	V_{IN}	GND - 0.7	VA + 0.7	V
Digital Input Voltage	(Note 3)	V_{IND}	-0.7	VDP + 0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes:

1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

DC ELECTRICAL CHARACTERISTICS

(GND = 0 V, all voltages with respect to ground. PSR_MCLK=12.288 MHz)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA	I_A	-	17.5	21	mA
(Normal Operation)	VDP = 5.0 V	I_D	-	22	26	mA
	VDP = 3.3 V	I_D	-	14.5	17	mA
Power Supply Current	VA	I_A	-	2	-	mA
(Power-Down Mode) (Note 4)	VDP = 5.0 V	I_D	-	2	-	mA
Power Consumption						mW
(Normal Operation)	VDP = 5.0 V		-	198	235	mW
	VDP = 3.3 V		-	135	161	mW
(Power-Down Mode)	VDP = 5.0 V		-	20	-	mW
ADC Power Supply Rejection Ratio (1 kHz)	(Note 5)	PSRR	-	65	-	dB
V_Q Nominal Voltage			-	2.5	-	V
Output Impedance			-	25	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
FILT+ Nominal Voltage			-	5	-	V
Output Impedance			-	18	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA

Notes:

4. Power Down Mode is defined as $\overline{\text{PSR\_RESET}}$ = Low with all clocks and data lines held static.
5. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VDP)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VDP)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_o = 100 µA	(% of VDP)	V_{OH}	70%	-	-	V
Low-Level Output Voltage at I_o = 100 µA	(% of VDP)	V_{OL}	-	-	15%	V
$\overline{\text{OVERFLOW}}$ Current Sink		$I_{OVERFLOW}$	-	-	4.0	mA
Input Leakage Current		I_{in}	-	-	±10	µA

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	°C
Junction to Ambient Thermal Impedance	θ_{JA}	-	70	-	°C/W

ANALOG CHARACTERISTICS

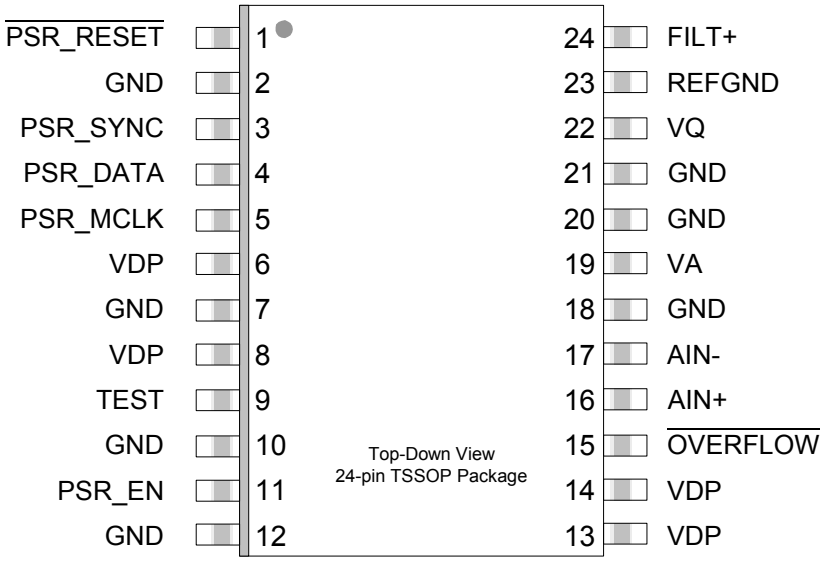
(Test conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Accuracy						
Gain Error				-	±5	%
Gain Drift			-	±100	-	ppm/°C
Analog Input Characteristics						
Full-scale Differential Input Voltage	-CZZ -DZZ		- -	1.13*VA 1.13*VA	- -	VPP VPP
AIN+/AIN- Input Range (VA = 5.0 V)	-CZZ -DZZ		1.1 1.1	- -	3.9 3.9	V V
Input Impedance (Differential)	(Note 6)		18	-	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

Notes:

6. Measured between AIN+ and AIN-

2. PIN DESCRIPTIONS



Pin Name	#	Pin Descriprion
VDP	6 8 13 14	**Digital Logic Power** (*Input*) – Digital core and input/output power supply. Nominally +3.3 V or +5.0 V. Supply decoupling should placed as close as possible to pin 6.
VA	19	**Analog Power** (*Input*) - Analog power supply. Nominally +5.0 V.
GND	2 7 10 12 18 20 21	**Ground** (*Input*) - Ground reference for both analog and digital.
$\overline{\text{PSR\_RESET}}$	1	**Reset** (*Input*) - When $\overline{\text{PSR\_RESET}}$ is low, the CS4461 enters a low power mode and all internal states are reset. On initial power up, $\overline{\text{PSR\_RESET}}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase.
VQ	22	**Quiescent Voltage** *(Output)* - Filter connection for the internal quiescent reference voltage.
REFGND	23	**Reference Ground** *(Input)* - Ground reference for the internal sampling circuits.
FILT+	24	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuit.
AIN+ AIN-	16 17	**Differential PSR Analog Input** *(Input)* - Signals are presented differentially to the delta-sigma modulator via the AIN+/- pins.
PSR_MCLK	5	**Master Clock** *(Input)* - Clock source for the delta-sigma modulator and output data.
PSR_SYNC	3	**Synchronization Data Output** (*Output*) - Used to synchronize the serial data in the PWM modulator.
PSR_DATA	4	**PSR Serial Data Output** (*Output*) - Power supply modulated and formatted serial data.
PSR_EN	11	**PSR Enable** (*Input)* - A high to low transition on this pin will enable the PSR feedback circuit.
$\overline{\text{OVERFLOW}}$	15	**Overflow** *(Output, open drain)* - Indicates a modulator overflow condition.
TEST	9	**Test** (*Output)* - This pin may toggle during normal operation and should be pulled low through a 47 kΩ resistor to GND in order to minimize noise.

3. TYPICAL CONNECTION DIAGRAM

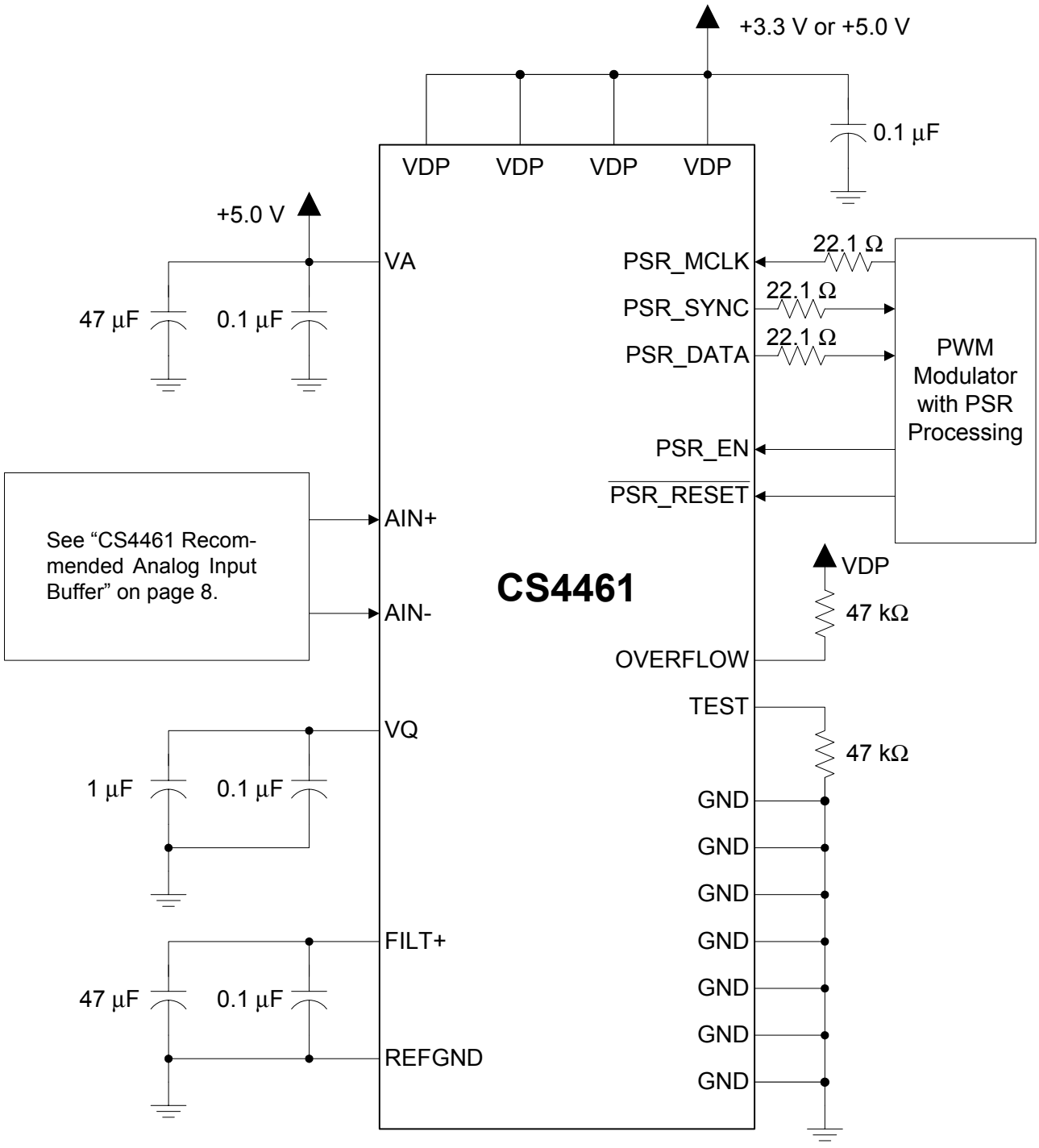


Figure 1. Typical Connection Diagram

4. APPLICATIONS

4.1 Digital Connections

PSR_MCLK provides the system clock for the CS4461. PSR_SYNC and PSR_DATA provide the output of the modulator to the class-D modulator with feedback capabilities. Series damping resistors should be used on PSR_MCLK, PSR_SYNC, and PSR_DATA to minimize noise. These should be placed as close as possible to their signal source. The pin labeled TEST should also be pulled low to GND through a 47 kΩ resistor to minimize noise coupling into the ADC modulator.

4.2 Analog Connections

The analog modulator samples the input at PSR_MCLK/4 (6.144 MHz with PSR_MCLK=24.576 MHz). Figure 2 shows the suggested analog input filter. This filter topology will correctly buffer the power supply's AC and DC components for PSR processing by the class-D modulator. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. C0G dielectrics should be used wherever possible. R1 and R2 should be used to scale VP (class-D amplifier high voltage power supply) to less than the CS4461 maximum AIN+/AIN- input voltage (3.9 V).

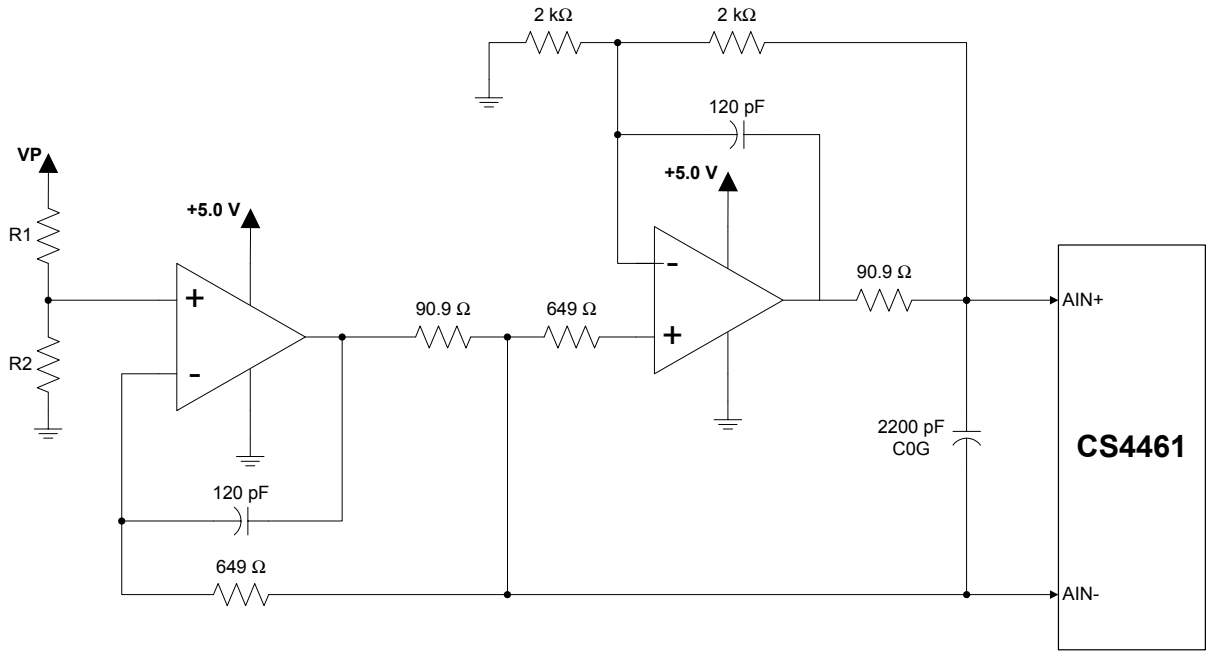


Figure 2. CS4461 Recommended Analog Input Buffer

The following equation can be used to scale R1 and R2:

$2 * (VP * (1 + \%_{VP\_Ripple})) * (R2 / (R1 + R2)) < 3.9\ V$

Example (VP = 40 V, $\%_{VP\_Ripple}$ = 4%):

2 * (40 * (1 + 0.04)) * (1.96 kΩ / (40.2 kΩ + 1.96 kΩ) = 3.87 V

4.3 Power-Up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies and clocks are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

The internal reference voltage must be stable for the device to produce valid data. Therefore, there is a delay between the release of reset and the generation of valid output, due to the finite output impedance of FILT+ and the presence of the external capacitance.

4.4 Overflow Detection

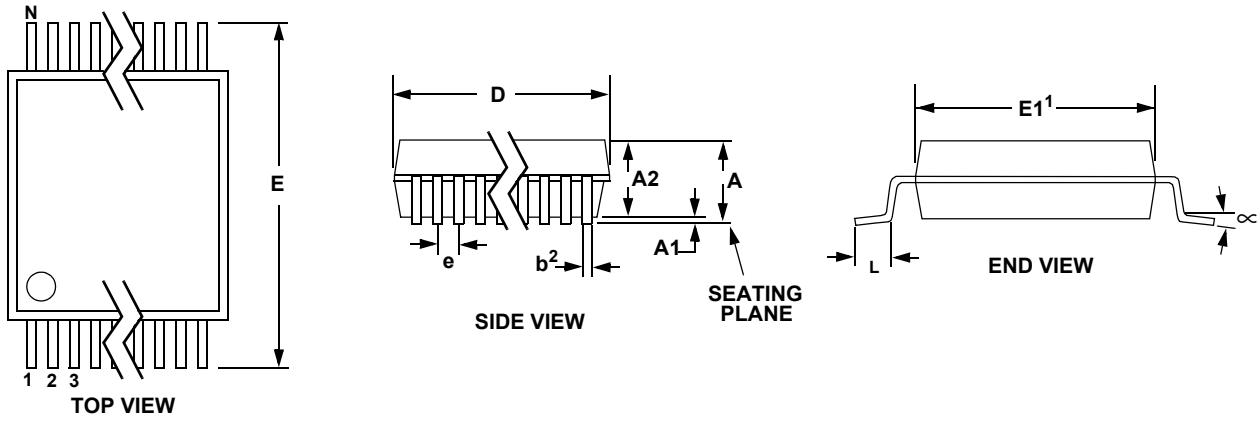
The CS4461 includes modulator overflow detection, indicated on pin 15, $\overline{\text{OVERFLOW}}$ (open drain, active low). $\overline{\text{OVERFLOW}}$ will go to a logical low as soon as an overrange condition is detected. The data will remain low until the condition is cleared.

4.5 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4461 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA and VDP connected to clean supplies. VDP, which powers the digital logic, may be run from the system logic supply or may be powered from the analog supply via a resistor. In this case, no additional devices should be powered from VDP. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulator. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ to GND. The CDB44800 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

5. PACKAGE DIMENSIONS

24L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.303	0.307	0.311	7.70	7.80	7.90	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
µ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes:

1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

6. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4461	Multi-bit A/D for Class-D Real-time PSR Feedback	24-TSSOP	YES	Commercial	-10° to +70° C	Rail	CS4461-CZZ
						Tape & Reel	CS4461-CZZR
				Automotive	-40° to +85° C	Rail	CS4461-DZZ
						Tape & Reel	CS4461-DZZR
CDB44800	Evaluation board for the CS44800/600 and the CS4461	-	-	-	-	-	CDB44800

7. REVISION HISTORY

Release	Date	Changes
A1	May 2004	1st Advance Release
F1	September 2005	Updated ordering information

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to **www.cirrus.com**